CLAIMS

What is claimed is:

1. A graphics processor, comprising:
a plurality of parallellized graphics computational units; and
one or more task allocation units programmed to bypass defective ones of said subunits within said groups, and to distribute incoming tasks only among operative ones of said subunits.

2. The graphics processor of Claim 1, wherein said parallellized graphics computational units include multiple vertex processors.

3. The graphics processor of Claim 1, wherein said parallellized graphics computational units include multiple vertex processors.

4. The graphics processor of Claim 1, wherein said parallellized graphics computational units include multiple texturing pipelines.

5. The graphics processor of Claim 1, wherein said parallellized graphics computational units include memory controllers.

6. An integrated circuit, comprising:
   a plurality of parallellized groups of identical processing subunits;
   task allocation units associated with ones of said groups; wherein said task allocation units are programmed to bypass defective ones of said subunits within said groups, and to distribute incoming tasks only among operative ones of said subunits;
   whereby defects which disable some but not all of said subunits in any one group are not necessarily fatal.

7. A method of 3D graphics rendering which comprises: using a task allocation unit and parallellized graphics computational units with relations as recited in Claim 1.